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(54) Log-polar signal processing.

(57) The invention relates to a method and an arrangement intended for radio communication systems and effective in digitalizing and subsequently processing numerically arbitrary radio signals. The signals are represented by composite (complex) vectors which have been subjected to disturbances in the system, such that information in the signals has been lost. This information is restored in its entirety when practising the present invention. For the purpose of solving this problem, the inventive digitalizing arrangement includes a multistage logarithmic amplifier chain (A) in which each stage is connected to a separate detector (D), the output signals of which are added in an adder. The adder output signals are then transmitted to a first A/D-converter (AD1) for digitalizing and converting the amplitude components of the signal. At the same time, the undetected signal from the saturated output stage in the amplifier chain is transmitted to a second A/D-converter for digitalizing and converting the phase components of the signal. The digital values obtained on the outputs of the AD-converters (AD1, AD2) are applied to different inputs of a digital signal processor (MP) for numerical processing of the pairwise received digital values in a manner such as to restore the complete vector characteristic of the signal.

Description

LOG-POLAR SIGNAL PROCESSING

TECHNICAL FIELD

The invention relates to an improved method and arrangement of apparatus for digitalizing and subsequently processing numerically radio signals in those instances when the levels of said signal can vary over a wide dynamic range and where the level values cannot be readily determined beforehand with the aid of sampling techniques.

BACKGROUND ART

It is always possible to represent an arbitrary radio signal as a sequence of composite (complex) vectors. The real and imaginary parts of the vector sequence correspond to bipolar amplitude modulation (double side band suppressed carrier AM) of a cosine and sine carrier wave respectively (quadrature carriers). When wishing to process a radio signal numerically using digital arithmetic implemented in either specific hardware logic or in software on a computer, microprocessor or some other programmable apparatus, it is first necessary to convert the signal in to numerical form with the aid of a A/D-converter (Analogue to Digital converter).

One common method of achieving this is to first resolve the radio signal into its real and imaginary complex vector part, by correlation with locally generated cosine and sine waves in two balanced mixers, and then to digitalize the two results by means of A/D-conversion. Sometimes there is used a variation of this technique, in which the radio signal is sampled pairwise, separated by one quarter period of its centre frequency. This so-called quadrature sampling technique combines the functions of sampling and A/D-conversion with resolution in real and imaginary parts.

DISCLOSURE OF INVENTION

The aforesaid, known solutions have practical limitations with respect to the possibilities of handling the dynamic ranges of the signals. Despite the absence of an input signal, the arrangement used in accordance with the first method, in which balanced mixers are used as correlators, does not necessarily produce a zero (0) volts, output signal. The output signal will typically have a D.C. off-set of some few millivolts or some tens of millivolts. At the same time, the acceptable, maximum signal level of the available supply voltage is limited to, for instance, +2.5 volts or, in the case of diode-ring mixers, perhaps to a still lower level of, for instance, +250 mV. The dynamic range for which the signal is, on one hand, much higher than the D.C. offset (mixer imbalance) and, on the other hand, lower than the saturation level, may be as small as 20 dB (decibel). This then requires the introduction of some form of automatic amplification control, in order to maintain the signal level of the mixer in the optimum range. In the case of a receiver which must necessarily accept random transmission of data in the form of bursts from different transmitters, it is not possible,

however, to predict the level of amplification required, when applying this method.

A further drawback, applicable to both of the aforesaid methods, resides in limited resolution during the A/D-conversion process. Assume that an A/D-converter is able to represent the whole of the signal level range. Further assume that the highest signal level may be equal to the supply voltage, e.g. 5 volts. An LSB-bit (Least Significant Bit) then corresponds to $5/256$ volts, i.e. approximately 20 millivolt. Consequently, a signal beneath 20 mV will remain totally undiscovered, while a signal of 320 mV will only be digitalized to a resolution of 4 bits, which is perhaps insufficient for subsequent signal processing. If a 4 bit resolution is nevertheless acceptable, the range in which the signals can be processed will be 16:1 or 24dB, which is a very poor dynamic range in the case of radio applications.

Radar receivers are typical examples of systems in which it is impractical to use automatic amplification control for the purpose of maintaining the receiver output within narrow limits, this impracticability being due to a number of unknown parameters, for instance such parameters as the distance to the reflecting object, the size of said object and the duration of the pulse. Because of this a radar receiver will normally operate with a chain of intermediate frequency amplifiers known as "logarithmic amplifiers". Such an arrangement comprises a plurality of sequentially saturating, cascade-connected amplifiers each being provided with an amplitude detector (rectifier) whose output signals are intended to be added together. The arrangement functions in the following manner: In the case of the weakest input signal levels, it is solely the detector which is located at the end of the chain which will receive a signal whose level of amplification is sufficient for the detector itself to produce an output signal. This ability increases with increasing input signal levels, until the amplifying stage concerned is saturated. At this stage, and with correct selection of amplification for each amplifying stage, the preceding amplifying stage in the chain will begin to receive a signal which is sufficiently strong for detection purposes and therewith takes over the contribution to the output signal. For each X dB increase in input signal level, where X is $20 \log 10$ of the voltage amplification in each stage, the saturation point is moved rearwardly one stage in the chain, the net detected output signal therewith increasing by one unit. The net detected output signal is thus followed by an approximately rectilinear relationship with the logarithm on the input signal level. The dynamic range for which this coincides is limited solely by the number of amplifying stages and the thermal noise. The method of digitalizing the detected output signal for subsequent numeric processing of the signal in an arrangement according to the foregoing is insufficient when handling arbitrary radio signals, since the complex vector nature of the arbitrary radio signal

will be lost in such a sequential detecting process.

The method and arrangement solving said problems are characterized by the patent claims and involve the introduction of a further digitalizing process which operates on the saturated output of the last amplifying stage in an amplifier chain in accordance with the foregoing, extracting the vector information which otherwise would be lost. This procedure is followed by a multiple of numeric operations on the two digital quantities, in order to restore the complete vector characteristic of the signal. This can be effected with the aid of hardware logic or with programmable digital signal processors (microprocessors). The inventive digitalizing arrangement, intended for processing composite signals having a large dynamic range, thus includes a logarithmic amplifying chain similar to the kind used in radar receivers and in which the detected output signal from the amplifier is digitalized in a first A/D-converter, whereafter a second A/D-converter digitalizes the angle or phase information of the signal. The phase information is retained by utilizing a carefully configured chain of saturating amplifiers, and is available on the saturated output of the last amplifier stage, at which point the signal has obtained a constant level and all variations in amplitude have therewith been eliminated. The exact method in which phase information is extracted in the form of a numeric quantity is not an objective of the present invention and will therefore not be described in this document.

The advantages afforded by the inventive method and inventive arrangement reside in the solution of a troublesome problem within the field of radio communications, in a technically uncomplicated manner, therewith achieving high precision at low costs.

BRIEF DESCRIPTION OF DRAWING

An arrangement according to the invention will now be described in more detail with reference to an exemplifying embodiment thereof illustrated in the accompanying drawing, in which

Figure 1 is a block schematic of the inventive arrangement, and

Figure 2 is a simplified, schematic illustration of one variant of an amplifier chain according to Figure 1.

BEST MODE FOR CARRYING OUT THE INVENTION

Described in the following is a novel method of digitalizing composite signals and an arrangement for carrying out the method. A complex number can be expressed either in cartesian (x,y) form or in polar (R, THETA) form. Translation between these two forms can be effected readily with the aid of the equations $X = R \cos(\text{THETA})$; $Y = R \sin(\text{THETA})$.

The log polar form (r, THETA) in which $r = \log(R)$ can be advantageously used as an alternative to the two forms aforesaid. The following transformation will then apply: $(x,y) = \exp(r + j \text{THETA})$; $r(\text{THETA}) = \log(x,y)$.

These equations show that when having a value on the logarithm of the amplitude of the complex vector (r) and a value on the angle (THETA) of the complex

vector, it is possible to restore the cartesian components of the complex vector when so desired.

The inventive digitalizing arrangement for complex signals having wide dynamic ranges utilizes the principle illustrated in Figure 1. The signal to be processed is converted to an appropriate intermediate frequency and then applied to the input IN of the first amplifier of an amplifier chain A. Said chain including a number of progressively detecting amplifiers.

Suitable, logarithmic amplifiers are available on the market, in the form of integrated circuits. Each stage of the aforesaid amplifier chain consists of one such circuit of the type SL521 A (Plessey Semiconductors). It is also possible to incorporate all amplifying stages in one single circuit, for instance a Signetics SA 604 circuit.

Connected to each of the output of respective amplifying stages is a detector (a rectifier) which has the form of a diode circuit and which is individual to respective stages. The detector outputs are all connected to a summation circuit S of type LF 157 A (National Semiconductors), in which the values from each detector circuit are summated and produced in the form of a summated signal of the output of the summation circuit. This output is connected to an input of a first rapid analogue/digital converter AD1, for instance a converter of type MP 7683 (Micropower Systems). The LOG-amplitude, quantized to N bits, is produced on the outputs of the A/D-converter and delivered to a first number of inputs of a digital signal processor MP. N must be large enough to cover the desired dynamic range in increments or steps which are sufficiently small for the application concerned. For example, if a signal variation range of 128 dB is to be covered and $N = 8$ bits, the size of the quantizing steps will be $128/28 = 0.5$ dB. Said steps size must be small enough to reduce the quantization noise to a level adapted to the application concerned. Quantization is a known technique which lies outside the concept of the present invention and which will not therefore be described in detail in this document.

The signal produced on an output C of the amplifying chain is so strongly amplified as it appears hardlimited (clipped), i.e. the amplifiers are so amplified that the signal is converted into a two-level signal, a square-wave of alternating high or low level. This signal retains the phase-angle information of the original signal when timing the transitions between the two signal levels. The exact method in which phase angle information is extracted in numeric form constitutes no part of this invention, but can for instance be effected with the aid of an appropriate phase detector which is operative to compare the limited square wave with a reference square wave and then to produce an analogue voltage which is proportional to the phase difference, subsequent to which it is necessary to digitalize the signal in an analogue/digital converter. The signal produced on the output C of the last amplifier stage is applied to an input of a second A/D-converter AD2, in which the phase information of the signal is quantized to M bits and transmitted from the outputs of the A/D-converter to a second

multiple of inputs on the digital signal processor MP. This processor may be of the type TMS 320 C 25 (Texas Instruments) or some corresponding processor. There can be used any microprocessor whatsoever which is capable of effecting the log-polar/cartesian transformation at a speed rapid enough for the application concerned, when this is the form required for further processing. The cartesian signal components are produced on the outputs of the microprocessor, as will be seen from Figure 1. In the case of the arrangement illustrated in Figure 1, it is necessary to limit the bandwidth of the amplifier chain, in order to prevent the generation of excessive noise. Consequently, propagation of the signal through the amplifier chain will be delayed, resulting in a continuous delay in the contribution from each of the detector steps. In order to prevent the introduction of disturbances in the case of rapid variations in signal amplitude, it may be necessary to correct for this relative delay prior to the summation of said values.

Since an important feature of the inventive arrangement resides in the digitalizing of momentary envelope changes in the signal, the aforesaid relative delay may be compensated by including in the system a delay line DL with taps at given time distances. Figure 2 shows such a delay line connected to the detector outputs of the amplifier chain. The taps T1-Tn can be adjusted automatically so as to compensate for the delay occurring in the amplifiers. The tap output signals are then summed and delivered to the first A/D-converter AD1. Examples of other compensation methods include the use of switched capacitors or some other CCD-technique (Charge Coupled Device). Alternatively, the output signals from each amplifier stage or groups of amplifying stages may be digitalized separately with the aid of sampling clock signals and the individual values then added together digitally. Timing of the synchronizing and sampling processes is effected in a known manner with the aid of system clock CL, indicated purely schematically in the drawing.

When applying known techniques, amplitude information is extracted very seldomly, and then only for the purpose of establishing the long-distribution quality of the signal and not with the intention of restore the vector characteristic of the signal, as is the intention with the inventive arrangement. As will be understood from the foregoing, in order to achieve this it is necessary to digitalize the signal amplitude and phase angle synchronously at the same sampling rate, and to keep the values together in pairs for each sample, with the intention of restoring completely the instantaneous, composite vector sequence of the radio signal for use in the continued processing of the signal.

Claims

1. A method for digitalizing in a radio communication system arbitrary radio signals represented by composite (complex) vectors which have been subjected in said radio system

to disturbances which cause information in the composite signals to be lost, said digitalization being effected in a manner such as to completely restore the signals influenced by said disturbances, characterized in that for the purpose of restoring said information upon simultaneous digitalization of a first part quantity of the signal, this part quantity being approximately proportional to the logarithm of the instantaneous signal amplitude, and a second part quantity relating to the instantaneous phase shift of the signal, the signals are subjected to a step-wise amplification and detection process, whereafter the detected signals are summated and the signal is digitalized in a first stage, in which the amplitude components of the signals are extracted; and in that at the signal, amplified but undetected, is at the same time digitalized in a second stage, in which the phase components of the signal are extracted; and in that the thus digitalized signal components are subjected pairwise to numeric processing for the purpose of restoring the complete, composite vector sequence of the arbitrary radio signals.

2. An arrangement for carrying out the method according to claim 1 for digitalizing in a radio communication system arbitrary radio signals represented by composite (complex) vectors which have been subjected in said radio system to disturbances which cause information in the composite signals, to be lost, said digitalization being effected in a manner such as to completely restore the information the signals influenced by said disturbances, characterized in that a multi-stage logarithmic amplifier (A) receives said radio signals on its input and amplifies said signals; in that each stage in the amplifier is connected to a separate detector circuit (D); in that the information obtained from each of the detector circuits is added in an adding circuit (S), the output of which is connected to the input of a first analogue/digital converter (AD1) for conversion of the amplitude components to an N-bit binary code; in that the radio signals in an amplified but undetected state are transmitted from the saturated output of the last amplifier stage to the input of a second analogue/digital converter (AD2) for conversion of the phase components to an M-bit binary code, whereafter the digital values obtained on the outputs of respective AD-converters (AD1, AD2) are applied to various arrays of inputs on a digital signal processor (MP) for numeric processing of the pairwise received digital values, such that the complete vector characteristic of the signal is restored.

3. An arrangement according to claim 2, characterized in that a delay line (DL) which can be tapped with the aid of taps (T1-Tn) is connected between the outputs of the detectors (D) and said addition circuit (S) such as to compensate for the delay occurring when the signals proceed through the logarithmic, multi-

stage amplifier/detector chain.

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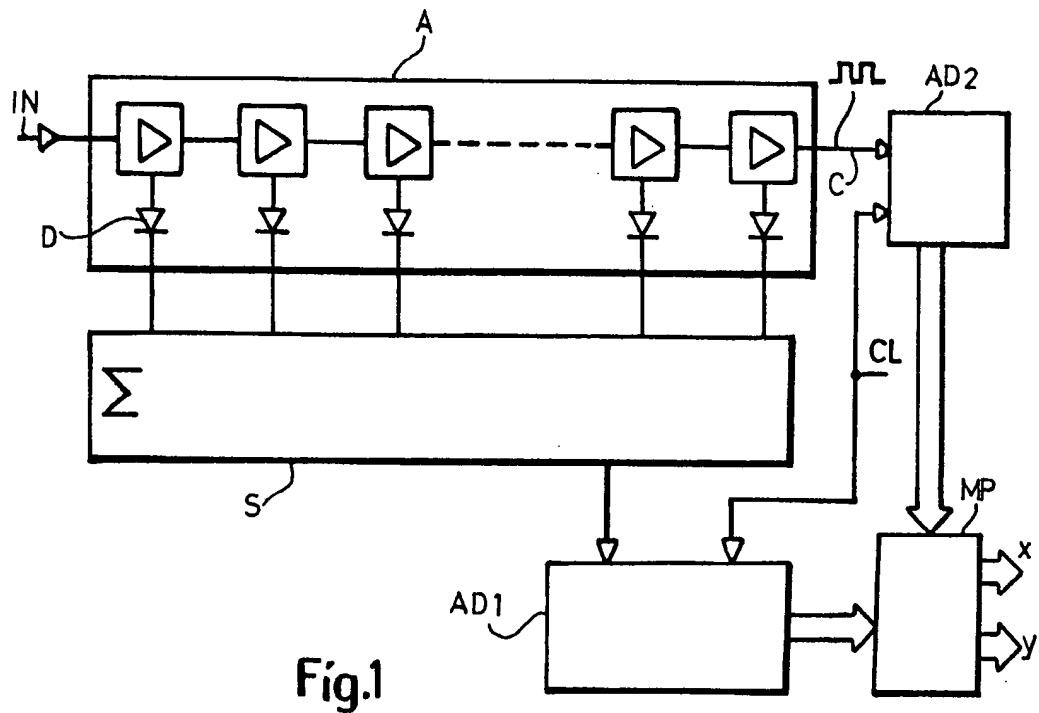


Fig.1

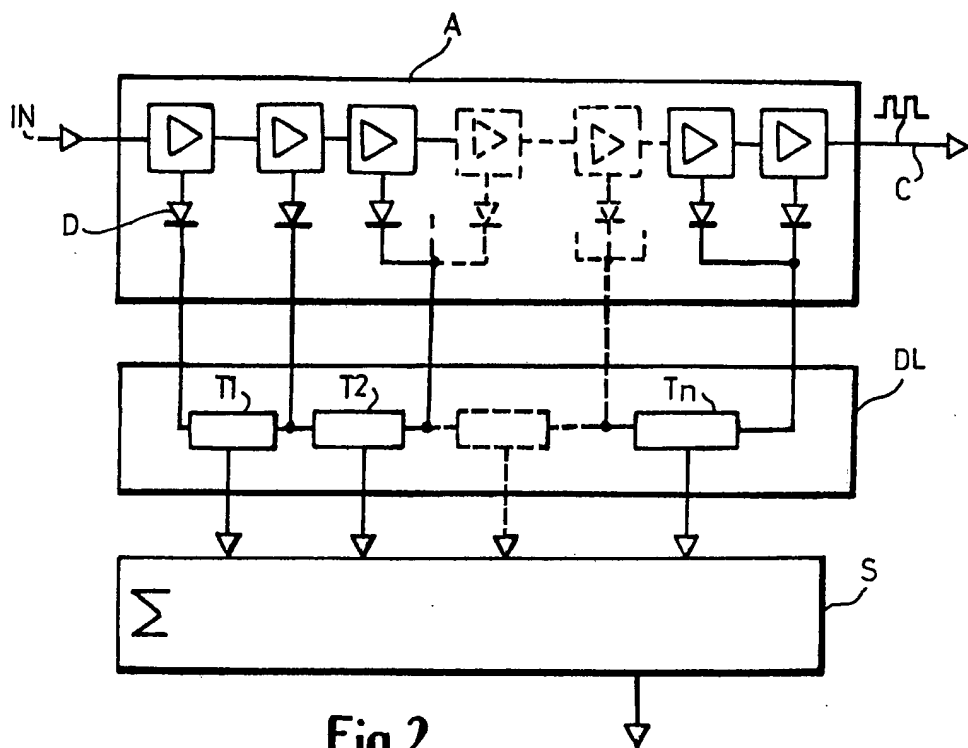


Fig.2



European Patent
Office

EUROPEAN SEARCH REPORT

Application number
EP 89850244.8

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
X	IEEE Journal of solid-state circuits, vol. SC-15, No. 3, June 1980, Barber and Brown, "A true logarithmic amplifier for radar applications" se*page 291, column 1, lines 21-25 (in order to...) and column 2 line 22- page 292, column 1, lines 1-7*. ----	1-2	H 04 L 27/06, H 03 D 1/00
A	EP-A2- 178 146 (PLESSEY OVERSEAS LTD) 16 April 1986 -----	1-3	
			TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
			G 01 R, H 03 D, H 03 M, H 04 L
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
STOCKHOLM		09-10-1989	JONSSON B
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	